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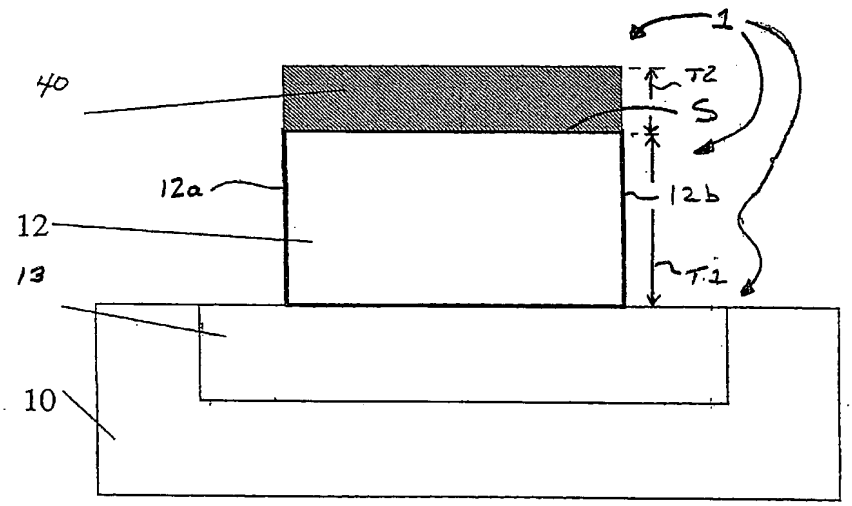
(54) Title: PROGRAMMABLE SEMICONDUCTOR DEVICE




(57) Abstract: A programmable device includes a substrate (10); an insulator (13) on the substrate; an elongated semiconductor material (12) on the insulator, the elongated semiconductor material having first and second ends, and an upper surface (S); the first end (12a) is substantially wider than the second end (12b), and a metallic material is disposed on the upper surface; the metallic material being physically migratable along the upper surface responsive to an electrical current (I) flowable through the semiconductor material and the metallic material.

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# Programmable Semiconductor Device

## Technical Field

The present invention relates to programmable semiconductor devices and, more particularly, to such devices usable as semiconductor electronic (E) fuses.

## Background Art

Semiconductor E-fuses in general are known. See, for example, U.S. Patent No. 5,334,880, Low Voltage Programmable Storage Element, issued August 2, 1994, by Abadeer et al., which is incorporated herein in its entirety.

However, known semiconductor E-fuses have not proven to be entirely satisfactory. Programming in silicon-based semiconductor devices (e.g., fuses) can result in post collateral damage of the neighboring structures. This result typically forces a fuse pitch, or fuse cavity, set of rules that do not scale well with the technology feature rules from one generation to the next. Thus, fuse density and effectiveness of fuse repair, replacement, or customization are limited. Typically, such damage is caused by particulates from fuse blow. In addition, standard electrical programming of a conductive fuse is to change its resistance, either from an unprogrammed state having a low resistance to a programmed state having a high resistance, or from an unprogrammed state having a high resistance to a programmed state having a low resistance. See, for example, USP 5,334,880. Such fuses contain an initial resistance, $R0 \pm \Delta R0$, and a programmed resistance, $Rp \pm \Delta Rp$. It is the $\pm \Delta Rp$ that causes fuse read instability because this parameter is statistical in nature. The variations that cause the R0 and Rp distributions to approach each other cause practical limitations in interrogating a programmed fuse through a standard CMOS latching circuit. To overcome these limitations, the prior art has included additional fuses as reference elements in order to discriminate

between a programmed and unprogrammed fuse. Such practices result in unwanted growth in the fuse bank area.

## Disclosure of Invention

The present invention overcomes this and other drawbacks by employing a device or fuse structure of a composite material that migrates during a programming event. The material that migrates (e.g., $WSi_2$) changes state, and does not cause collateral damage during its migration or material reformation, and has a programmed state where $\pm \Delta Rp$ is preferably equal to zero. This allows for individual fuses to discriminate among themselves and to eliminate unwanted reference fuse elements, as well as the circuitry used to bias and compare against the reference fuse elements.

According to the invention, a programmable device includes a substrate **(10)**; an insulator **(13)** on the substrate; an elongated semiconductor material **(12)** on the insulator, the elongated semiconductor material having first and second ends, and an upper surface **S**; the first end **(12a)** being substantially wider than the second end **(12b)**, and a metallic material **(40)** on the upper surface, said metallic material being physically migratable along the upper surfaces responsive to an electrical current **I** flowable through the elongated semiconductor material and the metallic material.

A method of programming a device includes flowing an electrical current **I** through a device having a semiconductor alloy **(40)** disposed on a doped semiconductor line **(12)**, for a time period such that a portion of the semiconductor alloy migrates from a first end **(12a)** of the device to a location **L** proximate to a second end **(12b)** of the device.

A method of fabricating a programmed semiconductor device, includes providing a semiconductor substrate **(10)** having a thermal insulator **(13)**; disposing an elongated semiconductor material **(12)** on the insulator, the semiconductor material having an upper surface **S**, a first resistivity, and two ends; disposing a metallic material **(40)** on the upper surface; the metallic material having a second resistivity much less than the first resistivity of

the semiconductor material; flowing an electrical current I through the semiconductor material **(12)** and the metallic material **(40)** for a time period such that a portion of the metallic material migrates from one end **(12a)** of the semiconductor material to the other end **(12b)** and melts the semiconductor material to form an open circuit **(90)**.

It is a principal object of the present invention to provide a programmable semiconductor device which does not cause collateral damage to adjacent devices or other elements during programming.

It is a further object of the present invention to provide a method of fabricating a programmable semiconductor device, which method is readily compatible with various standard MOS manufacturing processes.

It is an additional object of the present invention to provide a method of programming a programmable semiconductor device which reduces collateral damages to neighboring structures.

Further and still other objects of the present invention will become more readily apparent when the following detailed description is taken in conjunction with the accompanying drawings.

## Brief Description of Drawings

Fig. 1 is a side schematic view of a programmable semiconductor device according to one embodiment of the present invention.

Figs. 2-4 show top plan view photographs of devices according to the present invention when incompletely programmed (Fig. 2), completely programmed (Fig. 3) and overprogrammed (Figs. 4a, 4b, 4c).

Fig. 5a shows a top plan view photograph and Fig. 5b a side sectional view photograph

of a completely programmed device according to the invention.

Fig. 6 is a flow diagram of major steps to calibrate parameters for programming a device **(1)** of the invention.

Figs. 7-10 show preferred salient process steps for fabricating an unprogrammed device according to the invention.

Fig. 11a shows a top plan schematic views of the preferred embodiment of the device **(1)** according to the invention, and Fig. 11b shows the device **(1)** connected to an energy source for programming.

Figs. 12-15 are top schematic cross-sectional conceptual views into the direction of line AA, but rotated approximately 90° for easier explanation.

**Best Mode for Carrying Out the Invention**

Figure 1 shows a preferred programmable (un-programmed) semiconductor device **(1)** (e.g. fuse) in cross section. The fuse **(1)** includes an elongated semiconductor material **(12)** having a metallic material **(40)** disposed on an upper surface **S**. The material **(12)** is disposed on/ over an isolation region **(13)** in a silicon substrate **(10)**. Preferably, the unprogrammed fuse includes N+ polysilicon (90nm height/thickness **T1**) **(12)** and $WSi_2$ (55nm height/thickness **T2**) **(40)**. The region **(13)** is, for example, filled with an insulator such as an oxide. The region **(13)** is, for example, a known shallow trench isolation (STI) region. The device **(1)** includes a first end **(12a)**, a second end **(12b)** and a central portion or link **(12c)** connecting the first end **(12a)** to the second end **(12b)**. Preferably, the link **(12c)** and the second end **(12b)**, together, form a "T"-shaped member (Fig. 2, and Figs. 11a, 11b).

According to an important feature of the present invention, the resistivity of the metallic material **(40)** is much less than the resistivity of the semiconductor line **(12)**. Preferably, the resistivity of the material **(40)** is in a range of approximately (±10%) 15 ohms

per square to approximately 30 ohms per square, while the resistivity of the line **(12)** is in a range of approximately 100 ohms per square to approximately 200 ohms per square.

Preferably, the resistivity of the material **(40)** and the line **(12)** combined is approximately 17 ohms per square to approximately 25 ohms per square.

During programming, i.e., under suitable current, voltage and time conditions, the material **(40)** migrates from the first end **(12a)** and the link **(12c)**, to a location "L" proximate to the second end **(12b)**, to accumulate and ultimately heat and melt the semiconductor material **(21)** at the location "L" to form an open circuit **(90)** (see Fig. 15) within or at the location "L".

Figures 2 through 4 show an initial calibration used in determining the programming current and time required to rule out wafer level process variations when establishing the initial programming conditions. Figure 2 shows an incomplete programming using 4.5V, 5mA for 25μS. Figure 3 shows a typical preferred complete programming event at 4.5V, 5mA for 250μS. An open circuit **(90)** was formed at a location **L** proximate to the second end **(12b)**. The programming window was found to be compliant between 150μS and 350μS for this given technology. It was further determined that the fuse power and time scale with the technology feature, affording an electrical fuse that is reusable at nano scale technology nodes. Figures 4a, b and c indicate various results of overprogramming , and the effect of tungsten available volume.

These figures 4a, b, c show the over programming at 4.7V, 5mA from 1mS, 2S, 4S. The tungsten silicide **(40)** continues to migrate until it is depleted. The polysilicon line **(12)** still melts at the hottest spot, similar to Figure 3, but in the case of overprogramming the tungsten silicide **(40)** forms a bridge over the program location, as well as causing stress and damage in the nearby isolation trench. Although the line resistivity has significantly changed due to the migration of the tungsten silicide, and the inventors believe also the dopant, this is not considered a realizable fuse. However, this places a design guideline for a volume of the fuse metallic silicide as compared to a volume of the fuse neck at the programming location to avoid this overprogramming situation. This guideline can be used to size the area of the

migrating terminal pad so as to eliminate the condition of excess metallic silicide. These conditions are technology dependent, and can be established at the onset of technology manufacturing. This implies a fuse test and evaluation process flow is an additional feature of this invention. The process flow is self-explanatory and is shown in Figure 6.

Figures 5a and 5b show the result of program calibration on a random E-fuse of the invention. Programming occurs as a three stage event. Initially, as a current **I** is passed from the cathode to the anode terminals, the $WSi_2$ **(40)** migrates between the two terminals, and is heated to approximately (±10%) 2160°C. The local heating of the underlying polysilicon line **(12 or 21)** from the $WSi_2$ **(40)** and the subsequent opening **(90)** of the $WSi_2$ shunted path to the N+ polysilicon only path results in the N+ polysilicon line opening **(90)** as shown in Fig. 5b and Fig. 15. Subsequent analysis of the E-fuse structure indicated the $WSi_2$ as designed transformed into pure W, and all material was conserved. Also, collateral damage is eliminated. The open circuit as shown in Figures 5a and 5b provides the correlated feedback required in the calibration programming previously described. It is important to have a shunted N+ polysilicon migratable fuse for two reasons: it allows for low current uniform heating of the entire polysilicon line, without the requirement of large programming devices; and the migration of a hot refractory metal assists in the final link opening and programming, without causing debris surrounding the fuse that might cause subsequent reliability failure.

For the preferred fuse dimensions referenced in Figure 11a, the optimum fuse programming cycle is: Voltage Source = 4.5V, I = 5mA, Time = 250μS ± 100μS. The heating of the metallic silicide **(40)** is approximately (±10%) 2160 degrees C. Under an electron wind, the metallic silicide **(40)** migrates as depicted in the following figures (12-15), resulting in the final fuse programming, i.e., the opening of polysilicon line **(21)** as physically shown in Figure 15. Nothing happens to the surrounding isolation oxide **(13)**. Locations 70, 71 represent the proposed physical model of the redistribution of the metallic silicide **(40)** while it is heated and migrated by the voltage source (Fig. 11) and current flow **I**.

GC = polysilicon,

CG = electrical contact to the polysilicon,

M0 = metal zero (first metal to pad connections), and

Notch (optional) = notch in polysilicon pad.

Figures 7-10 show preferred process steps for fabricating the preferred embodiment of the fuse shown in Figure 1.

The process of fabricating the fuse of Figure 1 will be well understood by those skilled in the art in view of the instant disclosure.

As shown in Fig. 7, provide a substrate **(10)** which is bulk silicon, silicon-on-insulator or any other suitable substrate. Mask and etch shallow trench isolation region **(11)** (STI), fill trench **(11)** with an oxide **(13)**, planarize (e.g., CMP) to a top silicon surface **(14)**, grow gate oxide **(12)** for proposed active devices **D** which typically would be formed with the fuse **(1)**. Devices **D** are, for example, MOS devices such as FETs.

In Fig. 8, dispose (e.g., deposit) polysilicon **(22, 21)** (doped N or P, or undoped). Pattern with a photoresist mask **(20)**, etch and define active **(22)** and fuse **(21)** regions. See, for example, U.S. Patent Nos. 4,229,502 and 4,309,224, which are incorporated herein by reference in their entireties.

In Fig. 9, form sidewall spacers **(30)** with a conventional dielectric material.

In Fig. 10, suitably implant **(41)** into proposed FETs **D** and into the polysilicon **(21)** - if not in-situ doped polysilicon. Form metallic silicide region **(40)** by conventional techniques such as deposition (thermal evaporation of $WSi_2$, sputter deposition, etc.). The metallic silicide **(40)** preferably is $WSi_2$, but can be $CoSi_2$, $TiSi_2$, $NiSi_2$ and others with like electrical and thermal properties. The fuse region is shown between the vertical dashed lines of Fig. 10. Suitable annealing steps can also be performed, and the spacers can be removed. See, for example, the book VLSI Technology, by Sze et al., (1988, 2nd edition, McGraw Hill) for discussions of various process steps, which book is hereby incorporated by reference.

Figure 11 shows top views of the fuse, showing the fuse link width equal to 0.196μm,

and a fuse link (central portion) length of 1.862μm. Of course, fuse link widths can be << 0.2μm, i.e., 1μm and below. It is important that all of the poly **(12, 21)** sits over the isolation **(13)**, such that a thermal path is directed towards heating the metallic silicide **(40)** during a programming event. Metallic silicide is migrated from the huge negative terminal source and flows to the positive source via an electron wind. The positive source area must be << than the negative source area to allow the silicide to recrystallize within the underlying poly, and to heat the poly uniformly at the recrystalline point **L** so as to break **(90)** the line **(12, 21)** through heating.

Figures 12-15 show top schematic conceptual views useful for understanding the programming process of the present invention. The silicide **(40)** is driven from the negative terminal and piles up at the positive terminal where the polysilicon is heated and subsequently forms an open circuit, where ΔRp=0. A cross section shows the recrystallization of the silicide near (proximate) the point of programming versus the original "skin" silicide layer **(40)** over the negative terminal. No damage of the surrounding oxide is evident. It is an important criterion that the resistivity of the metallic silicide **(40)** be << than that of the underlying polysilicon **(12, 21)**. The materials described as examples meet this criterion.

Any metallic silicide ($NiSi_2$, $CoSi_2$ as examples) will react in the same manner as the tungsten silicide cladding layer we describe; i.e., we can drive a silicide along/down the line and force it to melt/annihilate the polysilicon layer **(12, 21)** underneath it due to the increased temperature of the "piled" metallic layer **(71)**.

Figure 12 shows a top view in cross section through the fuse prior to programming, showing isolation oxide **(13)**, doped polysilicon **(21)**, and homogeneous silicide layer **(40)** as formed.

As shown in Figure 13, during programming, current **I** is driven through the fuse at a given voltage **V**. Current conducts primarily through the low resistance silicide layer, and the electron wind produced by the current migrates the silicide **(40)** towards the end of the link as shown by the absence of the silicide on one end of the line **(70)** and the buildup of the silicide at the far end of the line **(71)**. The total volume of silicide is conserved within the line. Silicide

continues to react with the polysilicon at the end of the line.

Figure 14 shows, just prior to final programming, the migrated silicide **(71)** that consumes the entire end of the polysilicon line where the surrounding polysilicon is heated beyond its respective melting point. Current continues to flow, and silicide continues to migrate.

In Figure 15, programming is accomplished by removing the applied voltage and current, and the fuse link polysilicon **(12, 12c)** is pulled back into the migrated silicide **(71)**, forming, in effect, an electrical open circuit **(90)**.

To summarize: a low resistance layer **(40)** directly in contact, or chemically reacted with, a polysilicon layer **(21)** under a current **I** drive cathode to anode is used subsequently to melt a polysilicon line **(21)** at a location **(90)** and, thus, form/program a permanent antifuse.

While there has been shown and described what is at present considered a preferred embodiment of the present invention, it will be readily understood by those skilled in the art that various changes and modification may be made therein without departing from the spirit and scope of the present invention which shall be limited only by the scope of the claims.

Industrial Applicability

The present invention has applicability as E-fuses that may be employed during chip production, or within a deployed system to repair failing circuitry, or to customize a hardware or software application.

What is claimed is:

1. A programmable device, comprising:

a substrate **(10)**;

an insulator **(13)** on said substrate;

an elongated semiconductor material **(12)** on said insulator, said elongated semiconductor material having first and second ends, and an upper surface **S**,

said first end **(12a)** being substantially wider than said second end **(12b)**, and

a metallic material on said upper surface, said metallic material being physically migratable along said upper surface responsive to an electrical current **I** flowable through said semiconductor material and through said metallic material..

2. The programmable device as claimed in claim 1,

further comprising an energy source connected to said elongated semiconductor material, for causing an electrical current to flow through said elongated semiconductor material and through said metallic material, and for causing said metallic material to migrate along said upper surface.

3. The programmable device as claimed in claim 1, wherein said elongated semiconductor material comprises a doped polysilicon.

4. The programmable device as claimed in claim 1, wherein said metallic material comprises a metallic silicide.

5. The programmable device as claimed in claim 1, wherein said metallic material is a metallic silicide selected from the group consisting of $WSi_2$, $NiSi_2$ and $CoSi_2$.

6. The programmable device as claimed in claim 1, wherein said first end comprises a plurality of integral triangular-shaped portions.

7. The programmable device as claimed in claim 1, wherein said second end comprises an oblong-shaped portion.

8. The programmable device as claimed in claim 1, wherein said metallic material is disposed on the entire upper surface of said elongated semiconductor material.

9. The programmable device as claimed in claim 1, wherein said metallic material is a semiconductor alloy.

10. The programmable device as claimed in claim 1, wherein said elongated semiconductor material is N+ polysilicon and said metallic material is $WSi_2$.

11. The programmable device as claimed in claim 1, wherein said elongated semiconductor material includes a central portion connecting said first end to said second end.

12. The device as claimed in claim 11, wherein said central portion has a maximum substantially uniform width of less than approximately one micron.

13. The device as claimed in claim 11, wherein said central portion has a length of less than approximately two microns.

14. The device as claimed in claim 11, wherein said central portion and said second end form a T-shaped member.

15. A method of programming a device, comprising:

flowing an electrical current at a voltage through a device having a semiconductor alloy disposed on a doped semiconductor line, for a time period such that a portion of the semiconductor alloy migrates from a first end of the device to a location proximate to a second end of the device.

16. The method as claimed in claim 15, wherein said step of flowing causes heating of the semiconductor alloy.

17. The method as claimed in claim 15, wherein said step of flowing further comprises migrating an amount of the semiconductor alloy to the location sufficient to melt the doped semiconductor line and to cause an open circuit.

18. The method as claimed in claim 15, wherein the time period is a time period within a range of approximately 150μS to approximately 350μS, and the electrical current is approximately five mA.

19. The method as claimed in claim 16, wherein said step of flowing causes heating of the semiconductor alloy to a temperature of approximately 2160°C.

20. The method as claimed in claim 15, wherein said voltage is 4.7 volts, said current is 5mA, and said time period is 250μS.

21. A method of fabricating a programmed semiconductor device, includes:

providing a semiconductor substrate **(10)** having a thermal insulator **(13)**;

disposing an elongated semiconductor material **(12)** on the insulator, the semiconductor material having an upper surface S, a first resistivity, and two ends;

disposing a metallic material **(40)** on the upper surface; the metallic material having a second resistivity much less than the first resistivity of the semiconductor material;

flowing an electrical current **I** through the semiconductor material **(12)** and the metallic material **(40)** for a time period such that a portion of the metallic material migrates from one end **(12a)** of the semiconductor material to the other end **(12b)** and melts the semiconductor material to form an open circuit **(90)**.

22. The method as claimed in claim 21, wherein the first resistivity is approximately equal to 10 times the second resistivity.

23. The method as claimed in claim 21, wherein the first resistivity is a substantially uniform resistivity in a range of approximately 100 ohms per square to approximately 200 ohms per square, and wherein the second resistivity is a substantially uniform resistivity in a range of approximately 15 ohms per square to approximately 30 ohms per square.

24. The method as claimed in claim 21, wherein a combined resistivity of the elongated semiconductor material and the metallic material is a substantially uniform resistivity in a range of approximately 17 ohms per square to approximately 25 ohms per square.

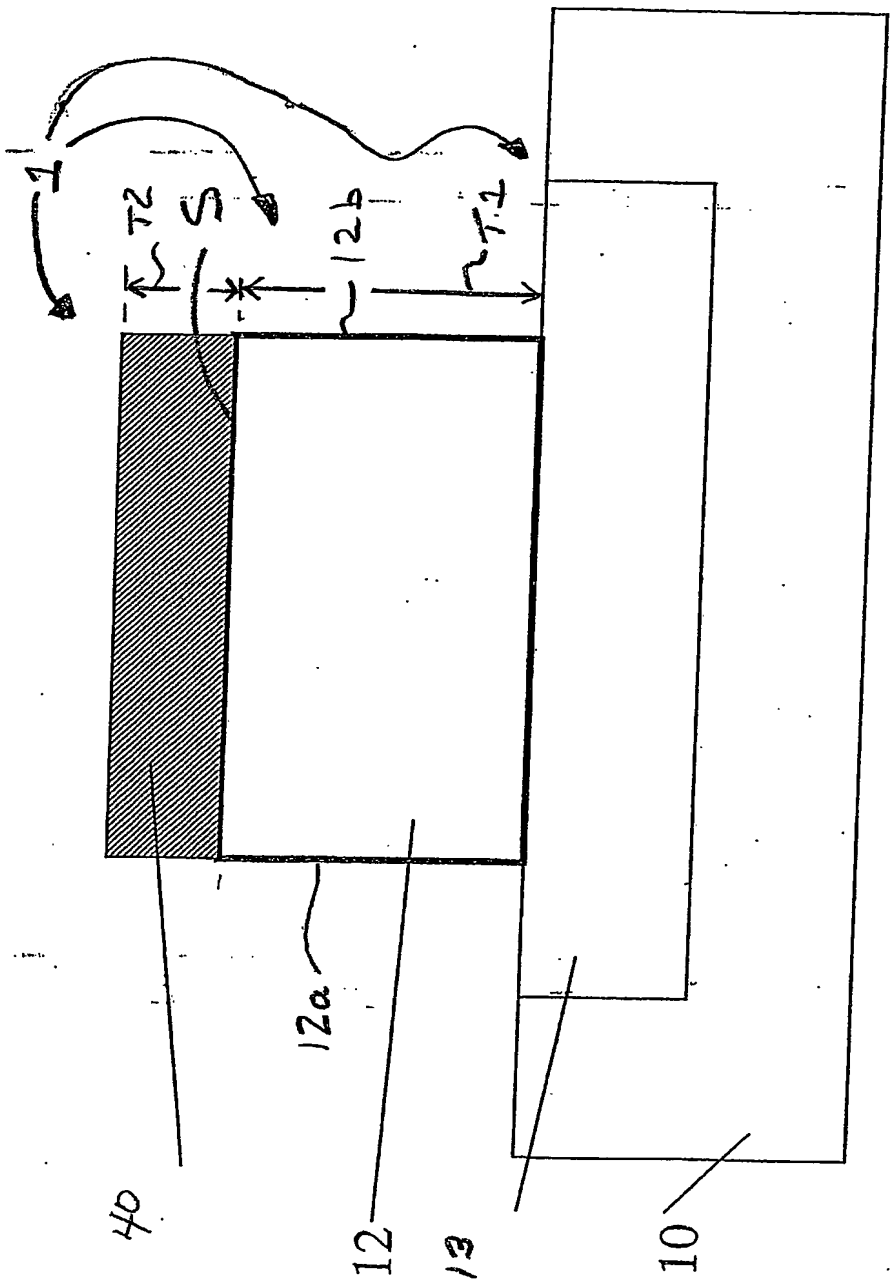



Figure 1;

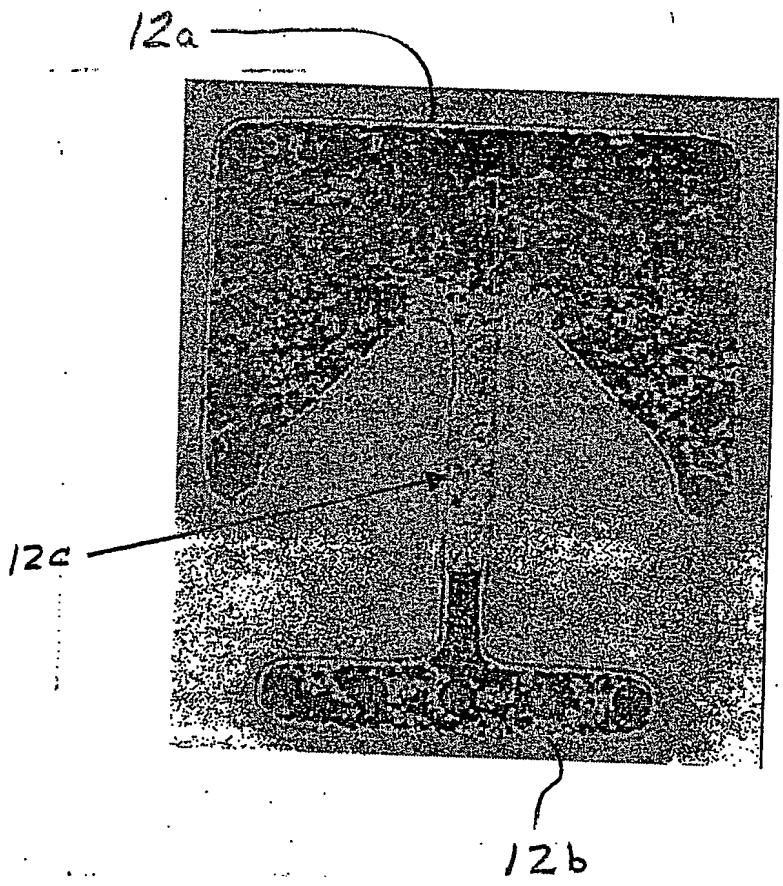



Figure 2:

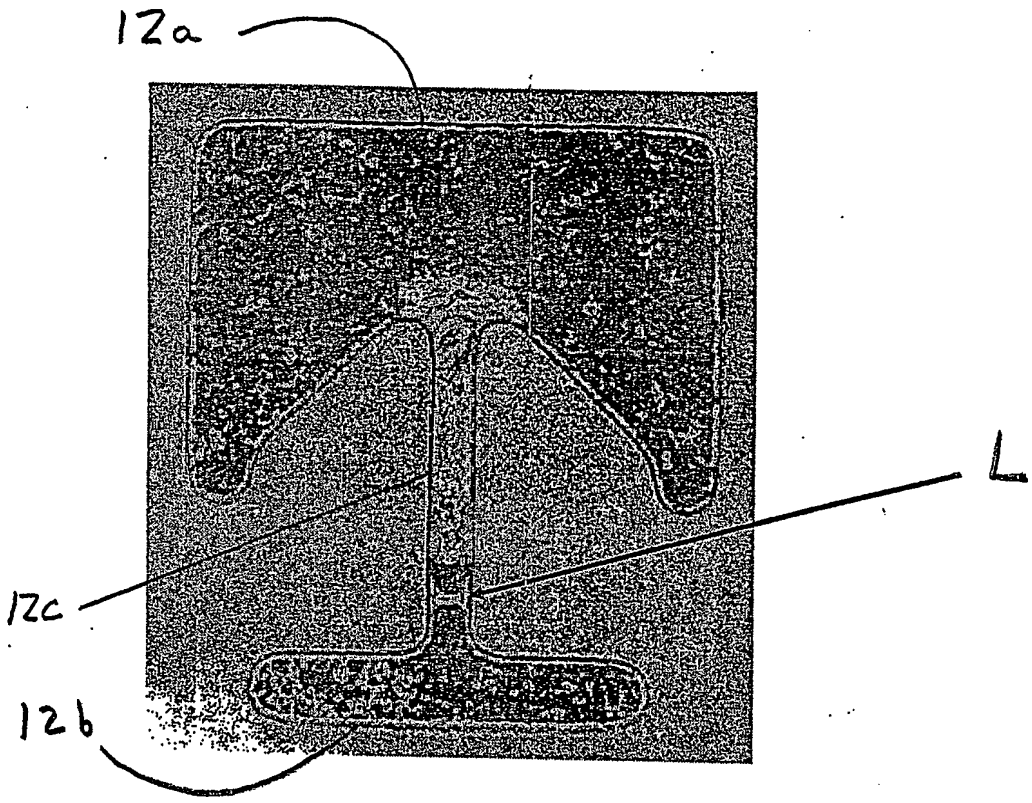



Figure 3:

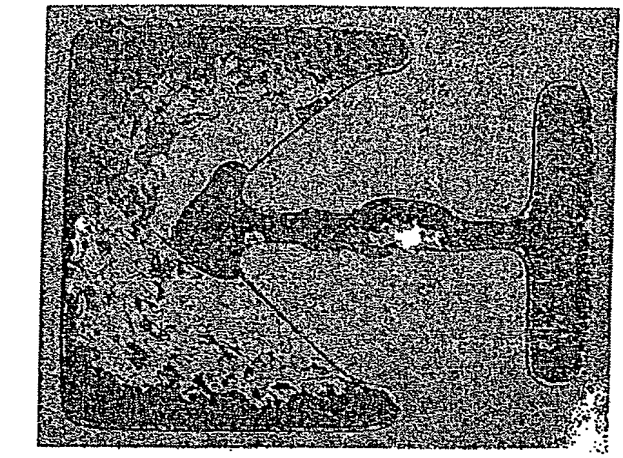


Fig. 4 (c)

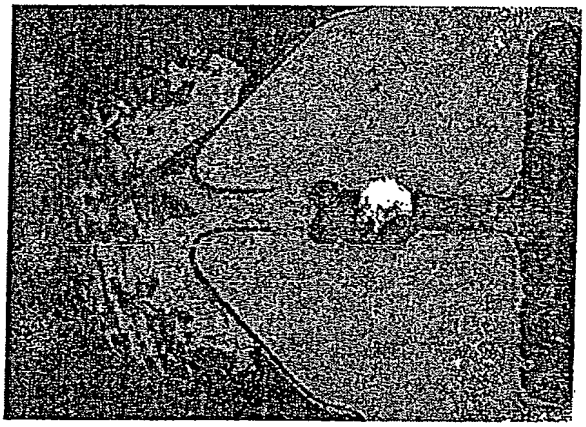


Fig. 4 (b)

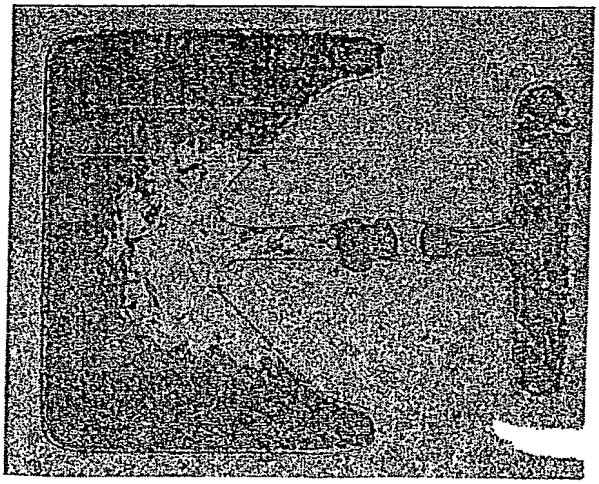


Fig. 4 (a)

Figure 4:

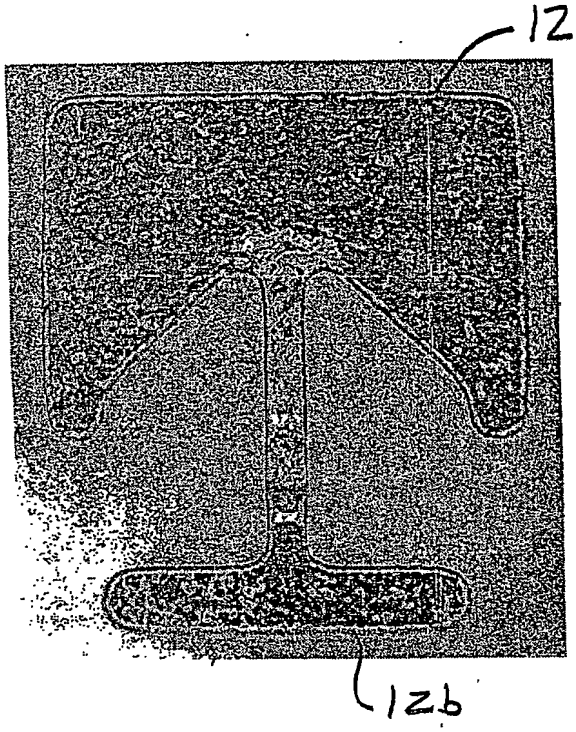



Fig 5 a

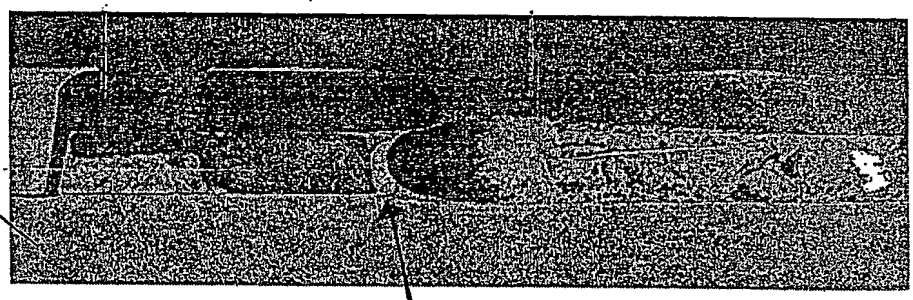



Fig 5 b

5/15

Figure 5:

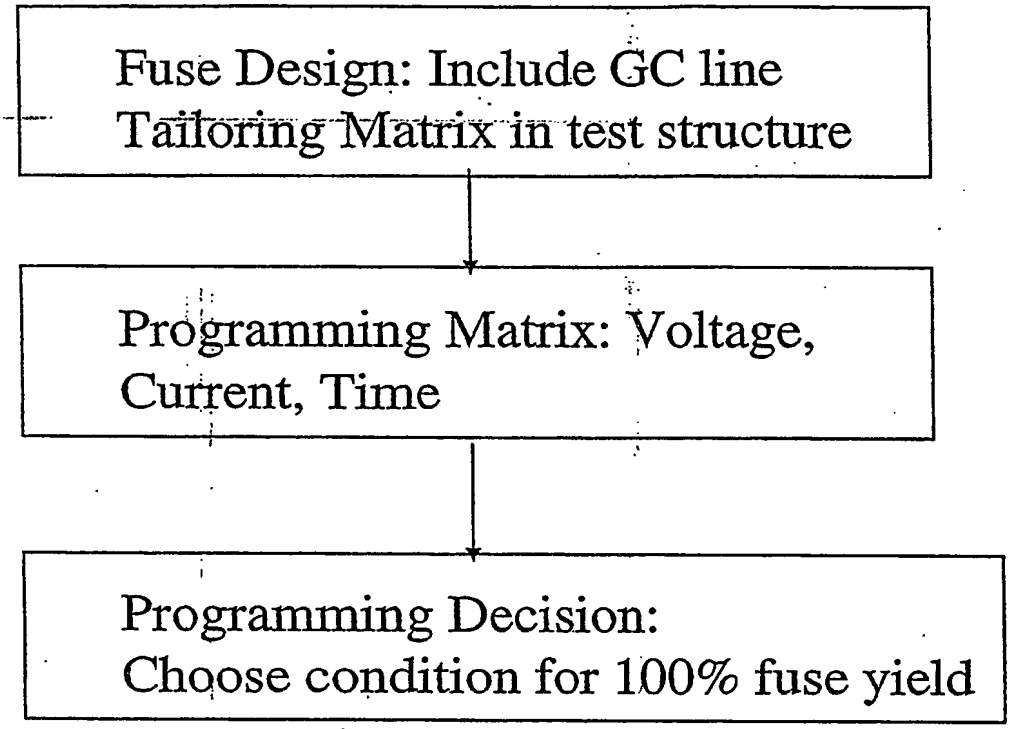
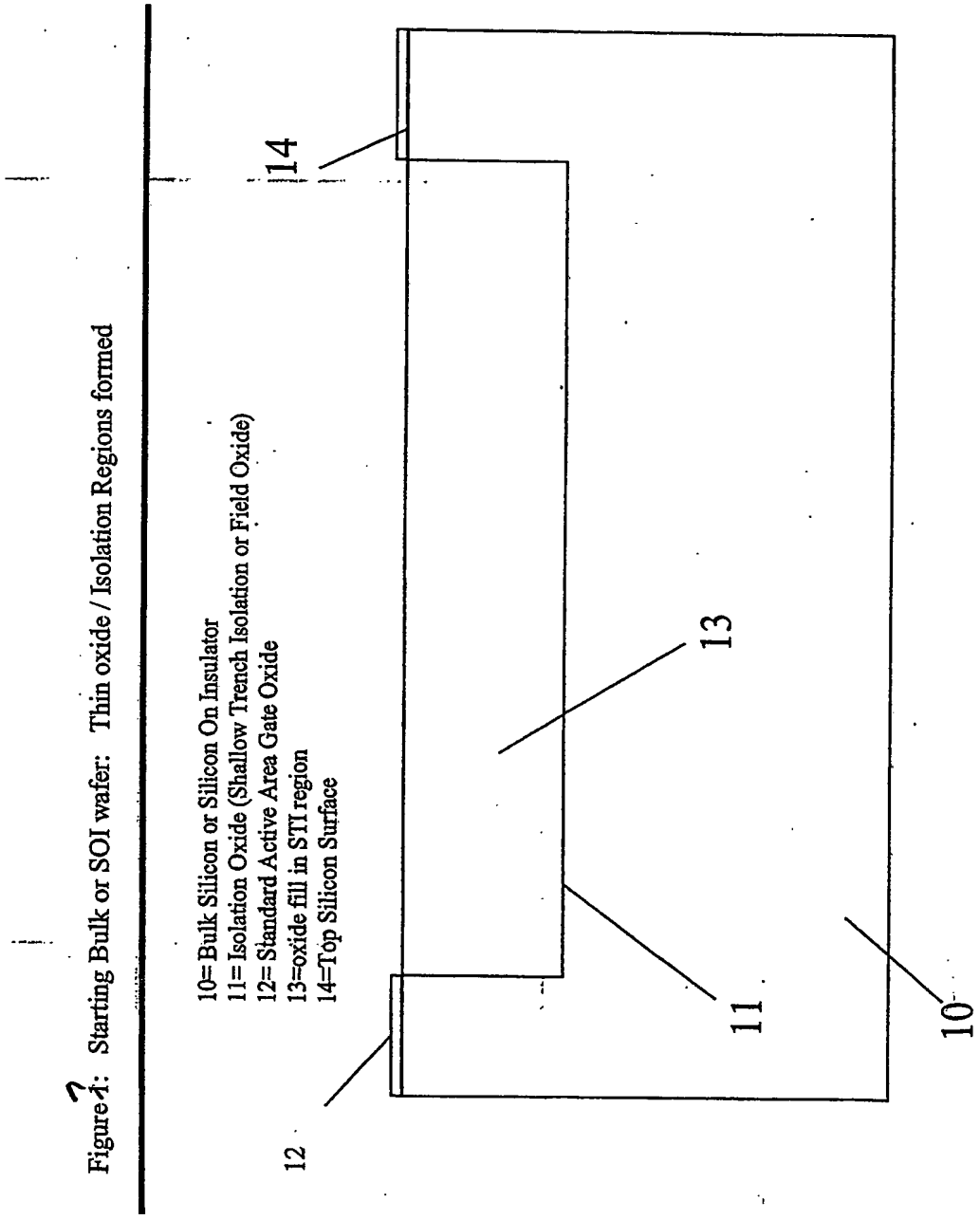

Fuse Design: Include GC line Tailoring Matrix in test structure
Programming Matrix: Voltage, Current, Time
Programming Decision: Choose condition for 100% fuse yield

Figure 6

Figure 1: Starting Bulk or SOI wafer: Thin oxide / Isolation Regions formed



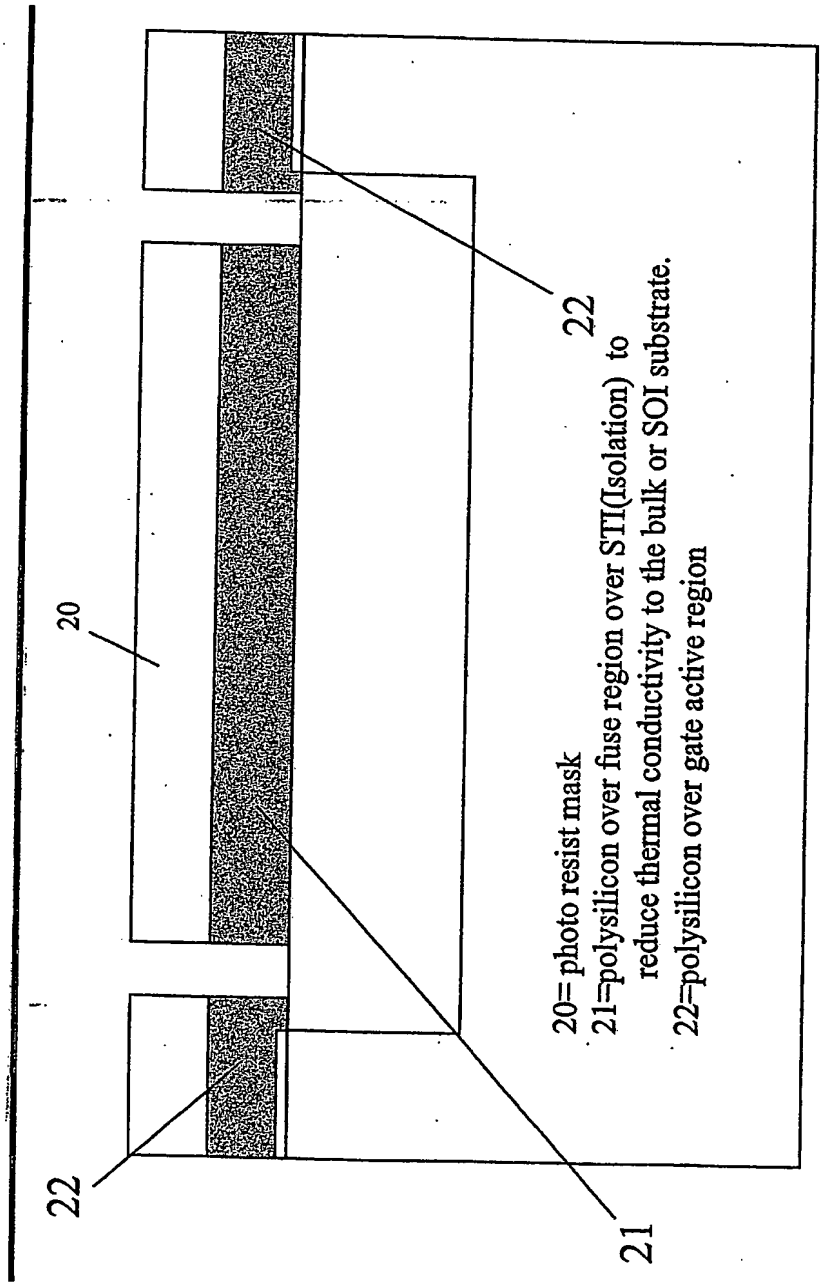



Figure 2: Deposit / Pattern Polysilicon

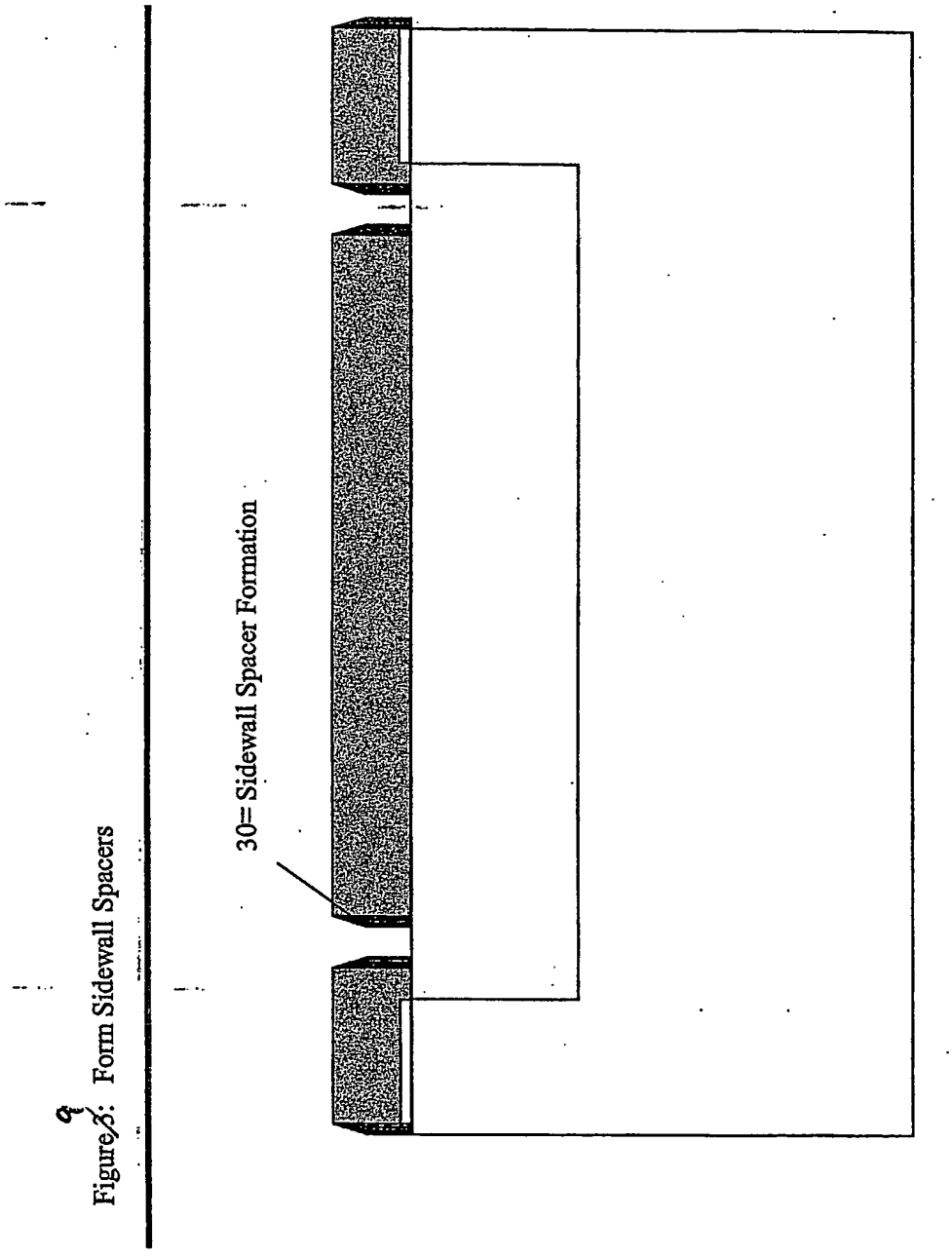



Figure 3: Form Sidewall Spacers

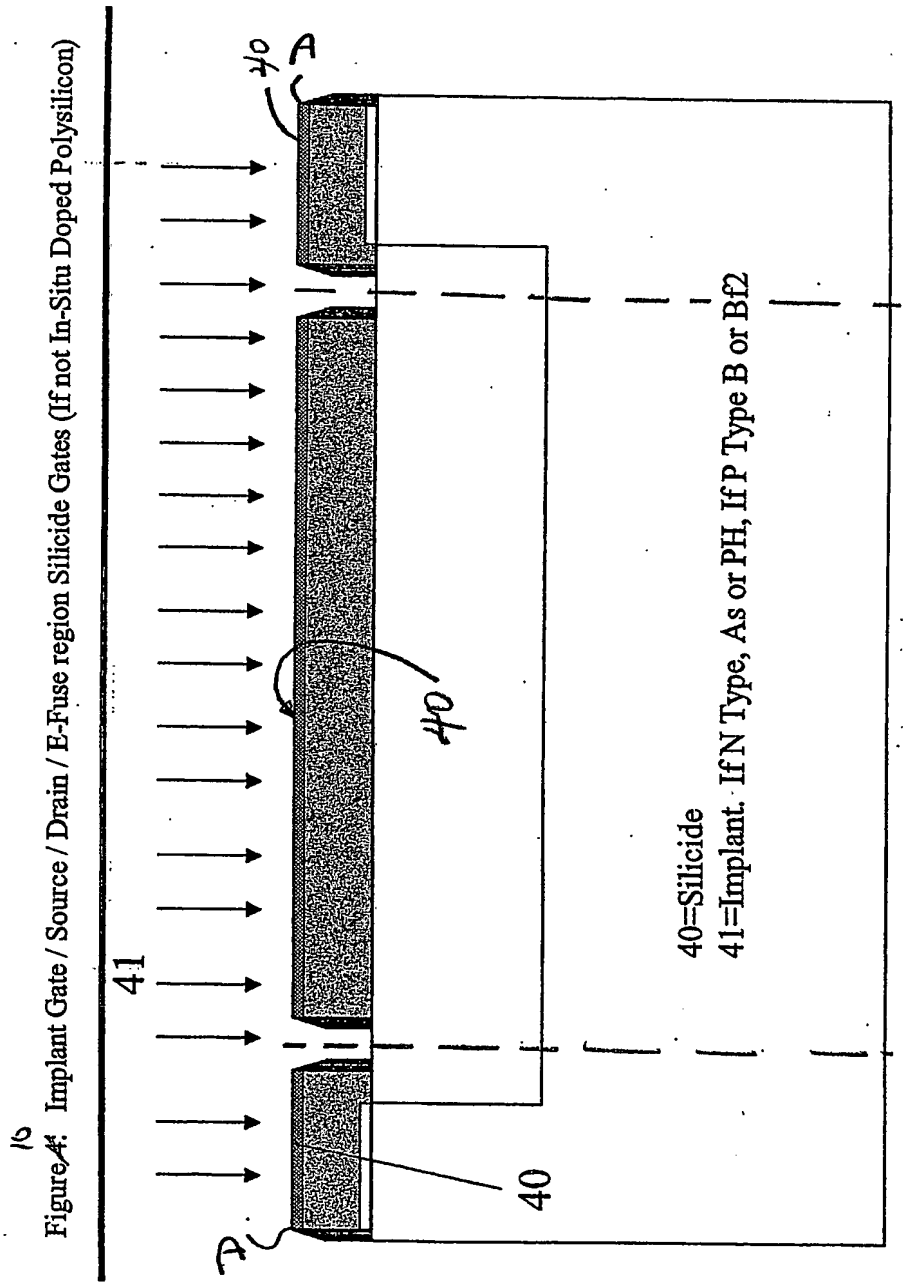



Figure 4: Implant Gate / Source / Drain / E-Fuse region Silicide Gates (If not In-Situ Doped Polysilicon)

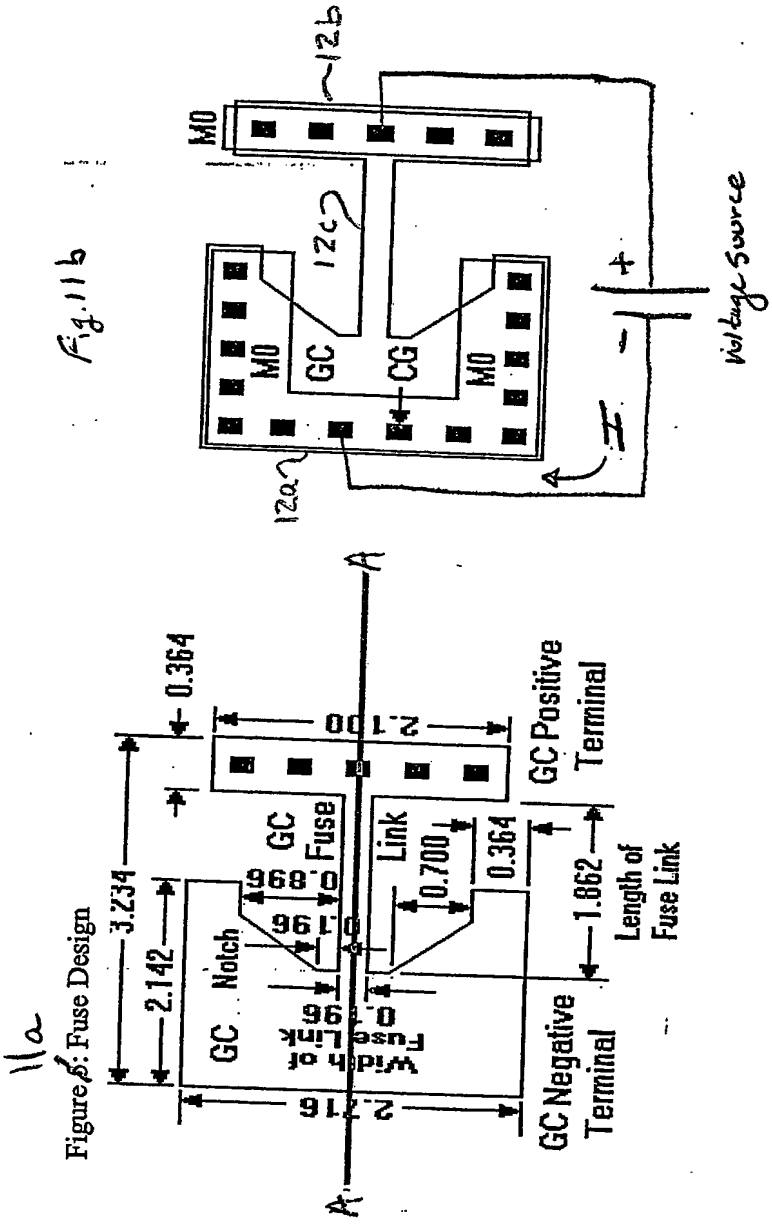



Fig. 11b

Figure 11a: Fuse Design

12
Figure 6: Fuse Cross Section A – A Prior to programming

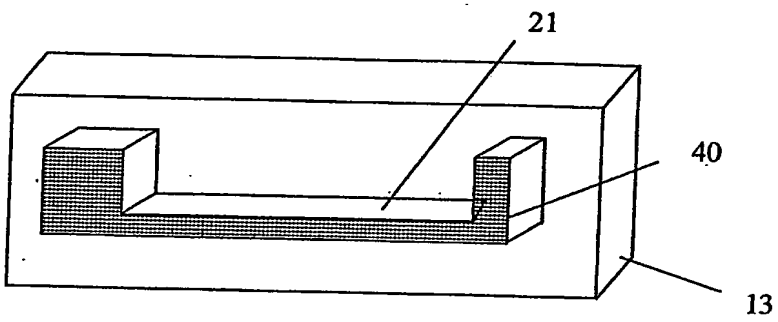


Figure 7: Fuse Cross Section A – A During Programming

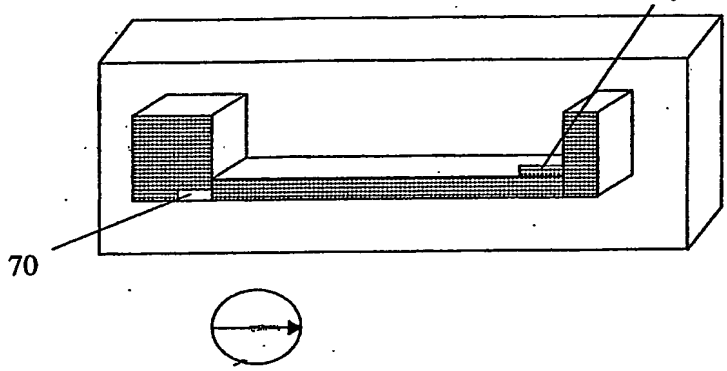


Figure 14: Fuse Cross Section A – A Just prior to programming

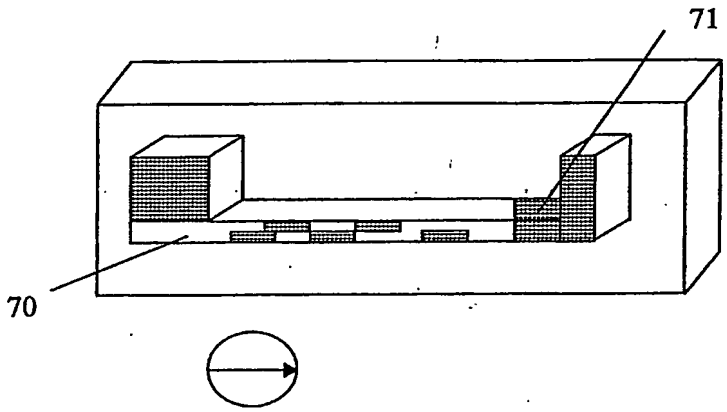
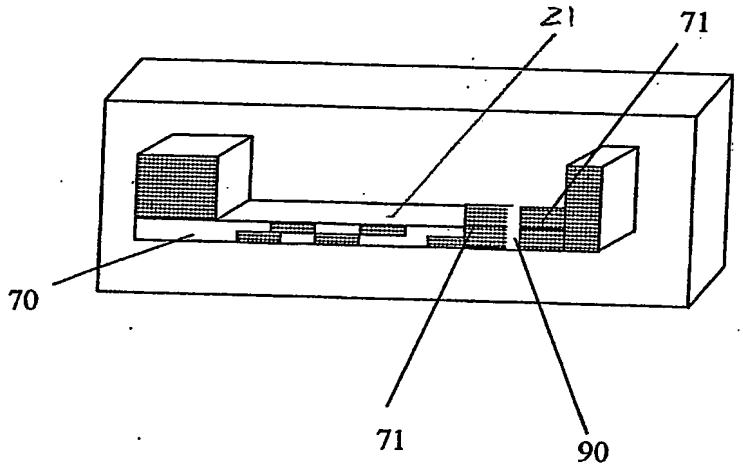


Figure 15: Fuse Cross Section A – A' Programmed device



# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/13392

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01L 29/00, 21/44
US CL : 257/530; 438/600, 467
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/530,529; 438/600, 467, 131

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 6,084,796 A (Kozicki et al.) 04 July 2000 (04.07.2000), Figures 5A and 5B. | 15-20 |
| --- | | --- |
| Y | US 6,433,404 B1 (Iyer et al.) 13 August 2002 (13.08.2002), Figure 3. | 1-14, 21-23 |
| A | US 6,418,049 B1 (Kozicki et al.) 09 July 2002 (09.07.2002), Figures 2A-2D. | 1-23 |
| T, E | US 2003/0094671 A1 (Stribley et al.) 22 May 2003 (22.05.2003), Figure 1. | 1-23 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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19 August 2003 (19.08.2003)

Date of mailing of the international search report
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